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10/633,712	08/05/2003	Jae-Hyun Kim	Q75787	6760

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SUGHRUE MION, PLLC
2100 PENNSYLVANIA AVENUE, N.W.
SUITE 800
WASHINGTON, DC 20037

EXAMINER	
MARTELLO, EDWARD	
ART UNIT	PAPER NUMBER
2628	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/633,712	KIM, JAE-HYUN	
	Examiner	Art Unit	
	Edward Martello	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 6 and 15 are objected to because of the following informalities: Both claims reference SRAM memory structures with dual "**porter**" and this should be changed to something similar to dual ported SRAM or SRAM with dual ports. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 3-10 and 12-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Cheung et al. (U. S. Patent 6,538,656 B2, hereafter '656).

3. Regarding claim 1, Cheung teaches a system on a chip (SOC) processor for multimedia ('656; video and graphics system implemented on an integrated circuit; fig. 40; col. 65, ln. 5-16), comprising: a pre-processor that converts an external image signal into a compressible signal ('656; fig. 40, video decoder, element 1636; col. 65, ln. 5-16); an encoder/decoder that generates compressed data by compressing the compressible signal, and codes the compressed data to produce a coded image signal('656; fig. 40, element 1654 VEC; col. 65, ln. 5-16); a post-processor that converts the coded image signal into a format for use by an image displaying apparatus ('656; fig. 40, video-graphics display and scale engine, element 1638); a graphic accelerator that processes three-dimensional graphic computation with respect to the image

signal output on the image displaying apparatus ('656; fig. 40, graphics accelerator, element 1624); a first system bus coupled to the encoder/decoder circuit unit ('656; fig. 40; memory controller input bus) ('656; fig. 40, internal- CPU-Register Bus); and a second system bus ('656; fig. 40, internal- CPU-Register Bus) coupled between the pre-processor, the postprocessor, and the graphic accelerator, wherein the first system bus and the second system bus communicate data to each other through a bridge DMA circuit unit ('656; DMA, element 1626; col. 66, ln. 52-56), and a controller controls said pre-processor, said encoder/decoder, said post-processor and said graphic accelerator ('656; fig. 40, video-graphics display and scale engine, element 1638).

4. Regarding claim 3, Cheung teaches the SOC processor of claim 1, wherein the graphic accelerator comprises: a geometry computation unit that performs geometry computation to display an object on the image displaying apparatus; and a rendering computation unit that performs rendering computation for visual representation of the object displayed on the image displaying apparatus with at least one of color, brightness and a design ('656; col. 66, ln. 37-51).

5. In regard to claim 4, Cheung teaches further teaches the processor as further comprising a texture/pixel cache configured to store 2-dimensional information of an object to be displayed and remove hidden surfaces of the image signal after three dimensional graphic processing ('656; col. 66, ln. 52-61).

6. Regarding claim 5, Cheung teaches the SOC processor of claim 4 and further teaches it as further comprising a buffer coupled between the controlling unit and the first system bus, wherein the buffer is capable of storing data for graphic to support the graphic accelerator ('656; fig. 40, Graphics Read, element 1622).

7. In regard to claim 6, Cheung further teaches wherein the buffer is implemented by using a static random access memory (SRAM) with a dual porter ('656; col. 66, ln. 52-61).

8. In regard to claim 7, Cheung teaches the SOC processor of claim 5 and further teaches wherein the buffer can receive data from an external memory having geometry information ('656; col. 66, ln. 52-61).

9. In regard to claim 8, Cheung further teaches wherein the external memory is a synchronous dynamic random access memory (SDRAM) ('656; col. 66, ln. 52-61) having a clock speed synchronized with that of the controlling unit ('656; fig. 40, memory controller, element 1634 - provides control to memory via Ctl in figure; col. 66, ln. 52-61).

10. Regarding claim 9, Cheung teaches the SOC processor of claim 7 and further teaches wherein the graphic accelerator receives the stored information by directly accessing the buffer ('656; fig. 40; col. 66, ln. 57-61).

11. In regard to claim 10, Cheung teaches a method of performing multimedia processing on a system on a chip (SOC) ('656; video and graphics system implemented on an integrated circuit; fig. 40; col. 65, ln. 5-16), comprising the steps of: converting an external image signal into a compressible signal ('656; fig. 40, video decoder, element 1636; col. 65, ln. 5-16); compressing the compressible signal to generate compressed data, and coding the compressed data to produce a coded image signal ('656; fig. 40, element 1654 VEC; col. 65, ln. 5-16); converting the coded image signal into a format for use by an image displaying apparatus ('656; fig. 40, video-graphics display and scale engine, element 1638); and processing three-dimensional graphic computation with respect to the image signal output on the image displaying apparatus ('656; fig. 40, graphics accelerator, element 1624); wherein said compressing is

performed in a circuit coupled to a first system bus ('656; fig. 40; memory controller input bus), and said converting steps and said processing step are performed in a circuit coupled to a second system bus, such that said first system bus and said second system bus ('656; fig. 40, internal-CPU-Register Bus) can operate at different respective clock frequencies, and wherein said first system bus and said second system bus communicate data to each other through a bridge DMA circuit unit ('656; DMA, element 1626; col. 66, ln. 52-56), and a controller controls said converting steps, said compressing step, and said processing step ('656; fig. 40, video-graphics display and scale engine, element 1638).

12. In regard to claim 12, Cheung teaches the method of claim 10 and further teaches wherein the processing comprises: performing geometry computation to display an object on the image displaying apparatus; and performing rendering computation for visual representation of the object displayed on the image displaying apparatus with at least one of color, brightness and a design ('656; col. 66, ln. 37-51).

13. Regarding claim 13, Cheung further teaches the method as further comprising storing 2 dimensional information of an object to be displayed, and removing hidden surfaces of the image signal after three dimensional graphic processing ('656; col. 66, ln. 52-61).

14. In regard to claim 14, Cheung further teaches the method as further comprising storing graphic data in a buffer to support the processing step ('656; fig. 40, Graphics Read, element 1622).

15. Regarding claim 15, Cheung further teaches wherein the buffer is implemented by using a static random access memory (SRAM) with a dual porter ('656; col. 66, ln. 52-61).

16. In regard to claim 16, Cheung teaches the method of claim 14 and further teaches wherein the buffer receives data from an external memory having geometry information ('656; col. 66, ln. 52-61).

17. Regarding claim 17, Cheung further teaches wherein the external memory is a synchronous dynamic random access memory (SDRAM) ('656; col. 66, ln. 52-61) having a clock speed synchronized with that of the controlling unit ('656; fig. 40, memory controller, element 1634 - provides control to memory via Ctl in figure; col. 66, ln. 52-61).

18. In regard to claim 18, Cheung teaches the method of claim 16 and further teaches wherein the stored information is received in a graphic accelerator for processing by directly accessing the buffer ('656; fig. 40; col. 66, ln. 57-61).

19. Regarding claim 19, Cheung teaches a computer readable medium configured for storing instructions to perform multimedia processing on a system on a chip (SOC) ('656; video and graphics system implemented on an integrated circuit; fig. 40; col. 65, ln. 5-16), said instructions comprising: converting an external image signal into a compressible signal ('656; fig. 40, video decoder, element 1636; col. 65, ln. 5-16); compressing the compressible signal to generate compressed data('656; fig. 40, element 1654 VEC; col. 65, ln. 5-16), and coding the compressed data to produce a coded image signal('656; fig. 40, element 1654 VEC; col. 65, ln. 5-16); converting the coded image signal into a format for use by an image displaying apparatus ('656; fig. 40, video-graphics display and scale engine, element 1638); and processing three-dimensional graphic computation with respect to the image signal output on the image displaying apparatus ('656; fig. 40, graphics accelerator, element 1624); wherein said compressing is performed in a circuit coupled to a first system bus, and said converting instructions and said

processing instruction are performed in a circuit coupled to a second system bus ('656; DMA, element 1626; col. 66, ln. 52-56), such that said first system bus and said second system bus can operate at different respective clock frequencies, and wherein said first system bus ('656; fig. 40; memory controller input bus) and said second system bus ('656; fig. 40, internal- CPU-Register Bus) communicate data to each other through a bridge DMA circuit unit ('656; DMA, element 1626; col. 66, ln. 52-56), and a controller controls said converting instructions, said compressing instruction, and said processing instruction ('656; fig. 40, video-graphics display and scale engine, element 1638).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

20. Claims 2, 11 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheung et al. (U. S. Patent 6,538,656 B2, hereafter '656) as applied to claims 1, 3-10, and 11-19 above.

21. In regard to claim 2, Cheung teaches the SOC processor of claim 1, but does not explicitly teach wherein a clock frequency of the first system bus is higher than a clock frequency of the second system bus. Cheung does teach that the first bus is a memory bus and the second is a CPU I/O & system bus. It would have been obvious to one of ordinary skill in the art at the time of the invention to design the first bus, the memory bus, to be the high speed bus that is handling all the graphics geometry and pixel data and to design the second bus to run at the slower rates encountered with CPU I/O and the like.

22. Regarding claim 11, Cheung teaches the method of claim 10 but does not explicitly wherein a clock frequency of the first system bus is higher than a clock frequency of the second system bus. It would have been obvious to one of ordinary skill in the art at the time of the invention to design the first bus, the memory bus, to be the high speed bus that is handling all the graphics geometry and pixel data and to design the second bus to run at the slower rates encountered with CPU I/O and the like.

23. In regard to claim 20, Cheung teaches the computer readable medium of claim 19 but does not teach wherein a clock frequency of the first system bus is higher than a clock frequency of the second system bus. It would have been obvious to one of ordinary skill in the art at the time of the invention to design the first bus, the memory bus, to be the high speed bus that is handling all the graphics geometry and pixel data and to design the second bus to run at the slower rates encountered with CPU I/O and the like.

Conclusion

The following prior art, made of record, was not relied upon but is considered pertinent to applicant's disclosure:

US 6570579 B1	Graphics display system - Single chip graphics system having integrated MPEG and graphical processors
US 5977997 A	Single chip computer having integrated MPEG and graphical processors

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edward Martello whose telephone number is (571) 270-1883. The examiner can normally be reached on M-F 7:30-5:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Xiao Wu can be reached on (571) 272-7761. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/EM/

Examiner, Art Unit 2628

/XIAO M. WU/
Supervisory Patent Examiner, Art Unit 2628